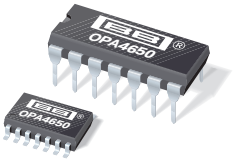
BURR - BROWN®



OPA4650

DEMO BOARD AVAILABLE

Wideband, Low Power, Quad Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- **LOW POWER: 50mW/channel**
- **UNITY GAIN STABLE BANDWIDTH: 360MHz**
- **FAST SETTLING TIME: 20ns to 0.01%**
- **LOW INPUT BIAS CURRENT: 5μA**
- **DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°**
- **14-PIN DIP and SO-14 SURFACE MOUNT PACKAGES AVAILABLE**

APPLICATIONS

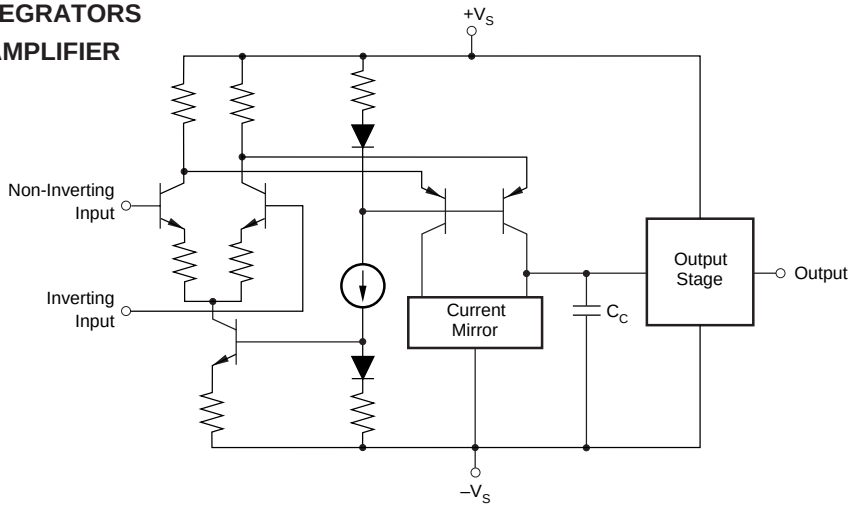
- **HIGH RESOLUTION VIDEO**
- **MONITOR PREAMPLIFIER**
- **CCD IMAGING AMPLIFIER**
- **ULTRASOUND SIGNAL PROCESSING**
- **ADC/DAC BUFFER AMPLIFIER**
- **ACTIVE FILTERS**
- **HIGH SPEED INTEGRATORS**
- **DIFFERENTIAL AMPLIFIER**

DESCRIPTION

The OPA4650 is a quad, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 360MHz as well as a 12-bit settling time of only 20ns. The low input bias current allows its use in high speed integrator applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA4650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA4650 is also available in single (OPA650) and dual (OPA2650) configurations.



Simplified Schematic
1 of 4 Channels

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SPECIFICATIONS

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

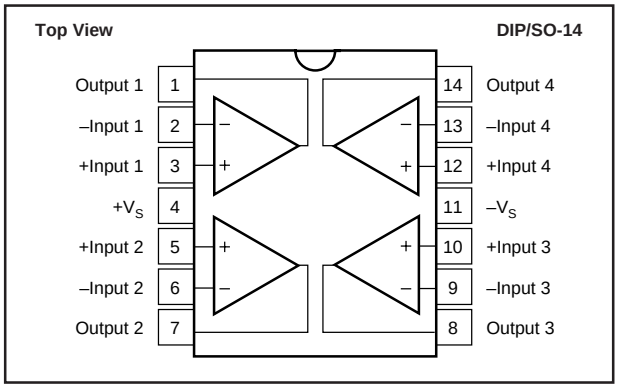
PARAMETER	CONDITIONS	OPA4650P, U MIN	OPA4650P, U TYP	OPA4650P, U MAX	UNITS
FREQUENCY RESPONSE					
Closed-Loop Bandwidth[1]	G = +1		360		MHz
	G = +2		120		MHz
	G = +5		35		MHz
	G = +10		16		MHz
Gain Bandwidth Product			160		MHz
Slew Rate[2]	G = +1, 2V Step		240		V/µs
Over Specified Temperature			220		V/µs
Rise Time	0.2V Step		1		ns
Fall Time	0.2V Step		1		ns
Settling Time 0.01%	G = +1, 2V Step		20		ns
0.1%	G = +1, 2V Step		10.3		ns
1%	G = +1, 2V Step		7.9		ns
Spurious Free Dynamic Range	G = +1, f = 5.0 MHz, V_O = 2Vp-p				
	R_L = 100Ω		68		dBc
	R_L = 402Ω		74		dBc
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.01		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.025		Degrees
Bandwidth for 0.1dB Flatness	G = +2		21		MHz
Crosstalk	Input Referred, 5MHz, all hostile		–63		dB
	Input Referred, 5MHz, Channel-to-Channel		–66		dB
OFFSET VOLTAGE					
Input Offset Voltage			±1	±5.5	mV
Average Drift			±3		µV/°C
Power Supply Rejection (+V_S)	$\|V_S\|$ = 4.5V to 5.5V	60	76		dB
(–V_S)		47	52		dB
INPUT BIAS CURRENT					
Input Bias Current	V_{CM} = 0V		5	20	µA
Over Temperature				30	µA
Input Offset Current	V_{CM} = 0V		0.5	1.0	µA
Over Temperature				3.0	µA
INPUT NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			43		nV/√Hz
f = 10kHz			9.4		nV/√Hz
f = 1MHz			8.4		nV/√Hz
f = 1MHz to 100MHz			8.4		nV/√Hz
Integrated Noise, BW = 10Hz to 100MHz			84		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1MHz to 100MHz			1.2		pA/√Hz
Noise Figure (NF)					
	R_S = 10kΩ		4.0		dBm
	R_S = 50Ω		19.5		dBm
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±2.8		V
Over Specified Temperature		±2.2			V
Common-Mode Rejection	V_{CM} = ±0.5V	65	90		dB
INPUT IMPEDANCE					
Differential			15 || 1		kΩ || pF
Common-Mode			16 || 1		MΩ || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	45	51		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	43			dB
OUTPUT					
Voltage Output					
Over Specified Temperature	No Load	±2.2	±3.0		V
	R_L = 250Ω	±2.2	±2.5		V
	R_L = 100Ω	±2.0	±2.3		V
Output Current, Sourcing		75	110		mA
Over Temperature Range		65			mA
Output Current, Sinking		65	85		mA
Over Temperature Range		35			mA
Short-Circuit Current			150		mA
Output Resistance	0.1MHz, G = +1		0.08		Ω
POWER SUPPLY					
Specified Operating Voltage			±5		V
Operating Voltage Range		±4.5		±5.5	V
Quiescent Current	All Channels		±23	±32	mA
Over Specified Temperature				±35	mA
TEMPERATURE RANGE					
Specification: P, U		–40		+85	°C
Thermal Resistance, θ_{JA}					
P			75		°C/W
U			75		°C/W

NOTES: (1) Frequency response can be strongly influenced by PC board parasites. The OPA4650 is nominally compensated assuming 2pF parasitic load. The demonstration board, DEM-OPA465xP, shows a low parasitic layout for this part. (2) Slew rate is rate of change from 10% to 90% of output voltage step.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage Across Device	11V
Internal Power Dissipation	See Thermal Considerations
Differential Input Voltage	±2.7V
Common-Mode Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, U,	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA4650U	SO-14 Surface Mount	235
OPA4650P	14-Pin Plastic DIP	010

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
OPA4650U	SO-14 Surface Mount	–40°C to +85°C
OPA4650P	14-Pin Plastic DIP	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

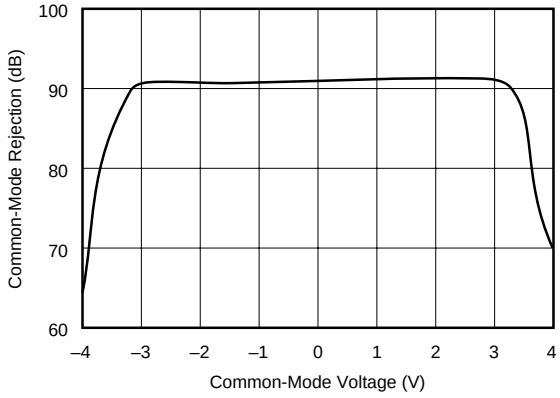
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

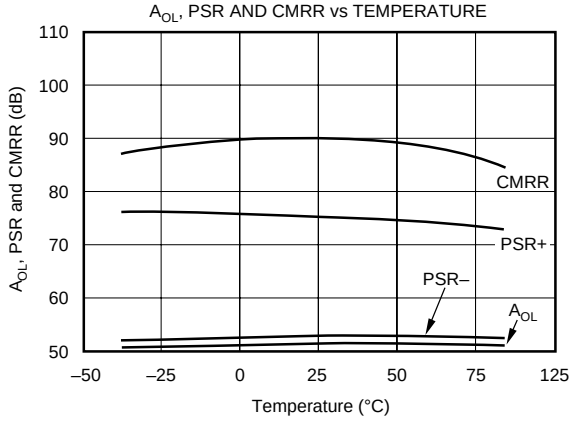
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

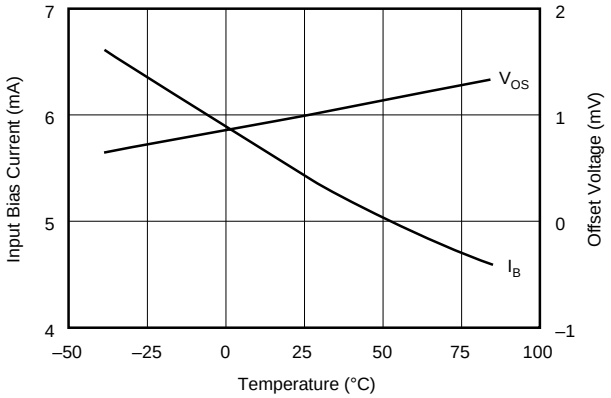
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



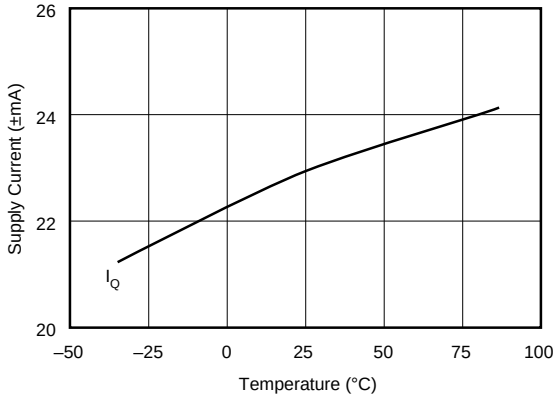
A_{OL}, PSR AND CMRR vs TEMPERATURE



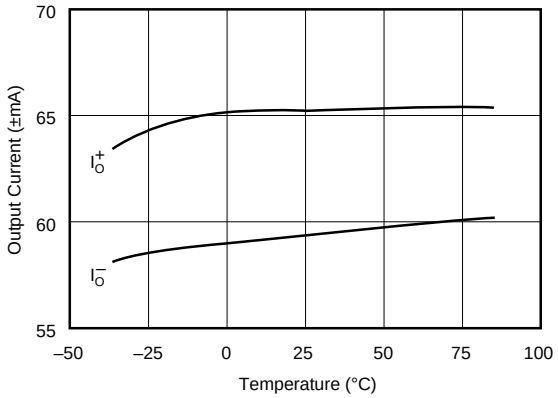
INPUT BIAS CURRENT AND OFFSET VOLTAGE
vs TEMPERATURE



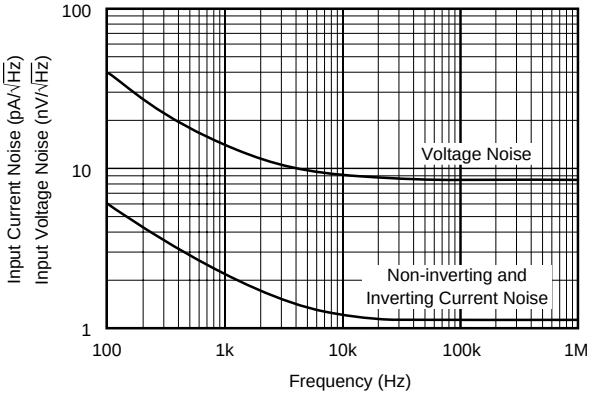
SUPPLY CURRENT vs TEMPERATURE



OUTPUT CURRENT vs TEMPERATURE



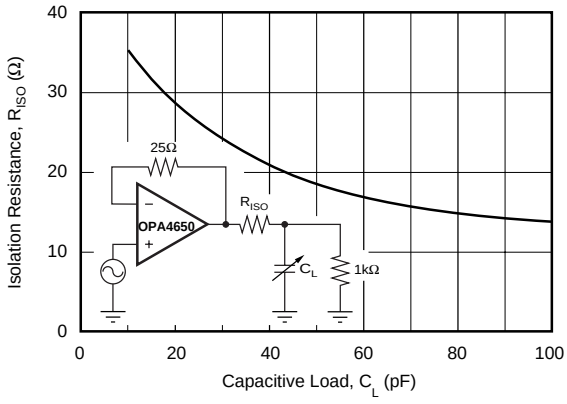
INPUT VOLTAGE AND CURRENT NOISE
vs FREQUENCY



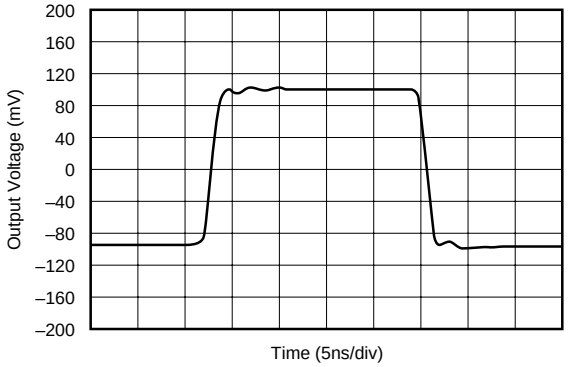
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

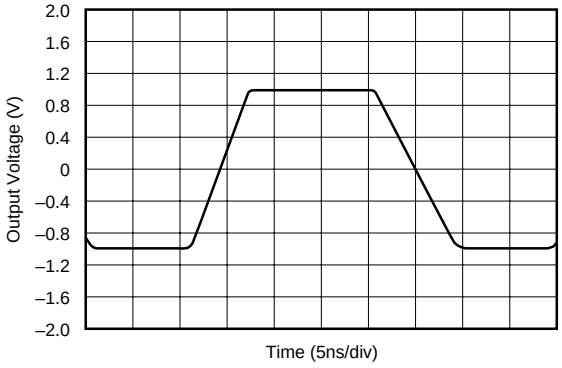
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



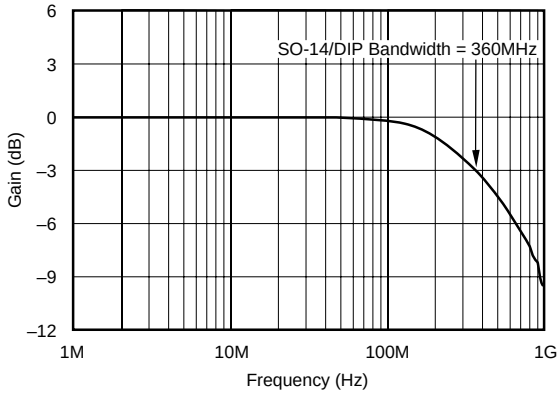
SMALL SIGNAL TRANSIENT RESPONSE (G = +1)



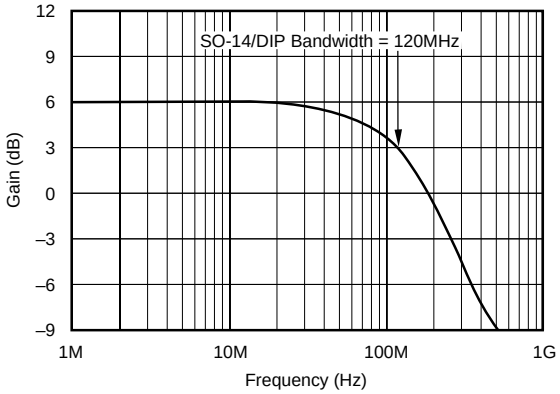
LARGE SIGNAL TRANSIENT RESPONSE (G = +1)



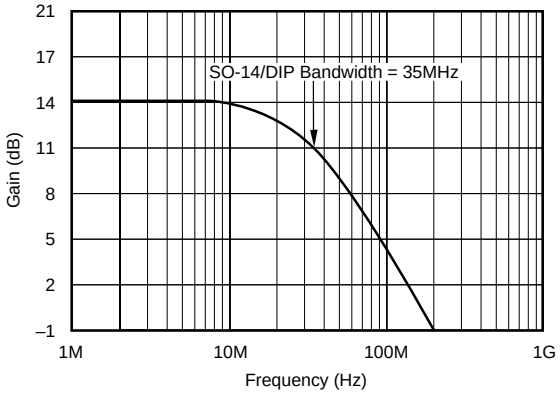
CLOSED-LOOP BANDWIDTH (G = +1)



CLOSED-LOOP BANDWIDTH (G = +2)



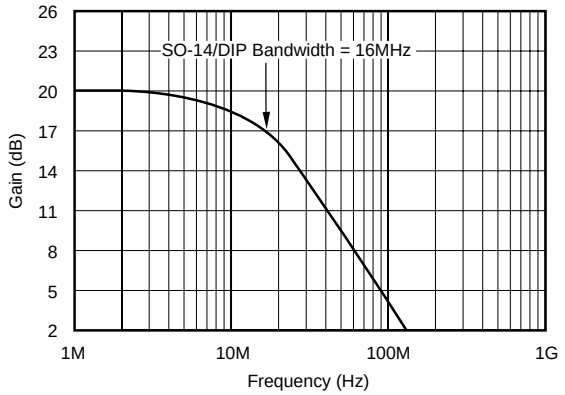
CLOSED-LOOP BANDWIDTH (G = +5)



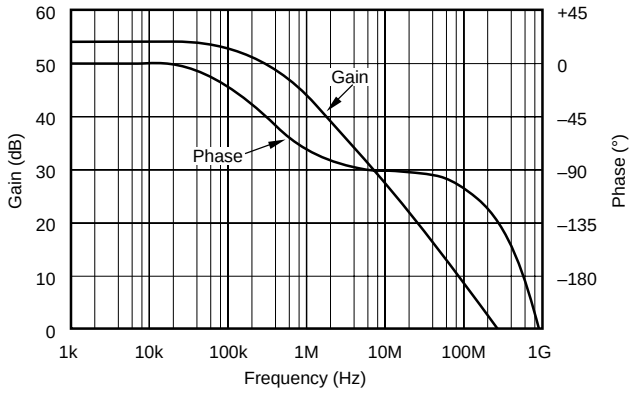
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

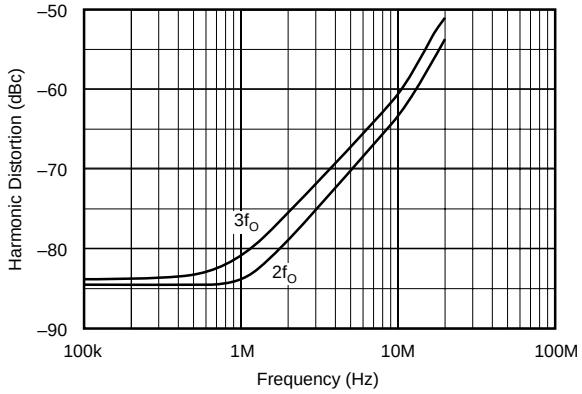
CLOSED-LOOP BANDWIDTH (G = +10)



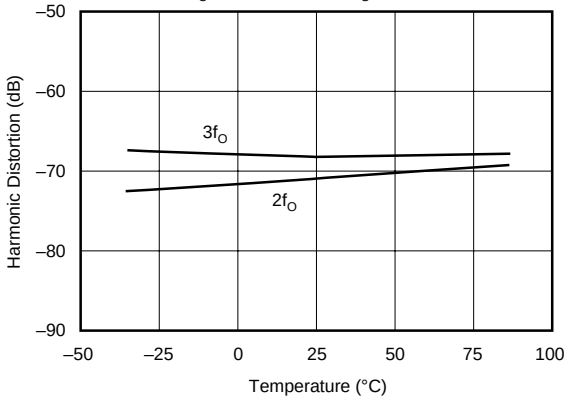
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



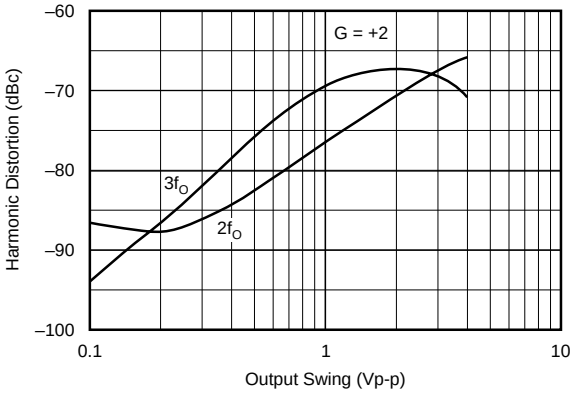
HARMONIC DISTORTION vs FREQUENCY (G = +1, V_O = 2Vp-p)



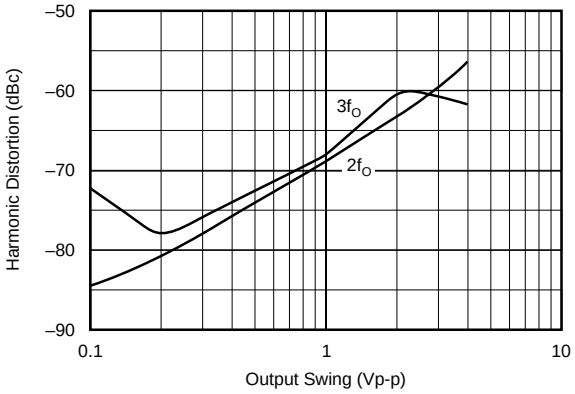
HARMONIC DISTORTION vs TEMPERATURE (f_O = 5MHz, G = +1, V_O = 2Vp-p)



5MHz HARMONIC DISTORTION vs OUTPUT SWING



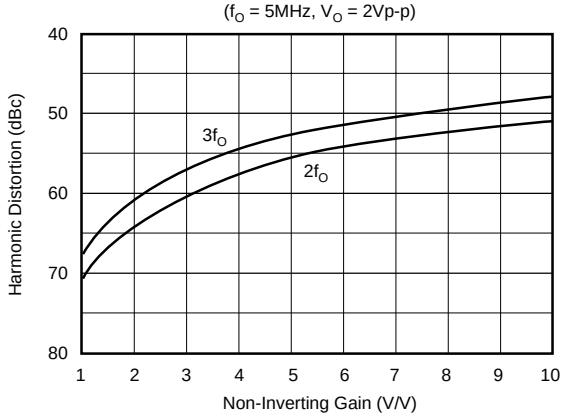
10MHz HARMONIC DISTORTION vs OUTPUT SWING



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

HARMONIC DISTORTION vs GAIN
(f_O = 5MHz, V_O = 2Vp-p)



DISCUSSION OF PERFORMANCE

The OPA4650 is a quad low power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA4650's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA4650 well suited for implementing filter and instrumentation designs. As a quad operational amplifier, OPA4650 is an ideal choice for designs requiring multiple channels where reduction of board space, power dissipation and cost are critical. Its ac performance is optimized to provide a gain bandwidth product of 160MHz and a fast 0.1% settling time of 10.3ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low dc input offset of ±1mV and drift of ±3µV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the quad current feedback OPA4658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA4650 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA4650. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Surface mount feedback resistors directly adjacent to the output and inverting input pins work well for the quad pinout. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting the resistor, excessively high resistor values can create significant time constants and degrade performance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this adds a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for a unity gain follower. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA4650 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA4650 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost

impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

The OPA4650 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

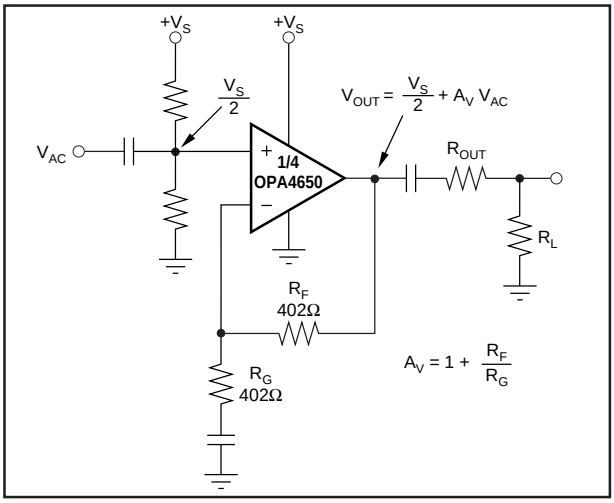


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

One simple way to null the initial offset voltage while retaining the low offset drift of the OPA4650 is shown in Figure 2. The 20kΩ potentiometer and the 47kΩ series resistor R_{TRIM} create a small correction current which is summed into the inverting node. The 0.1µF capacitor keeps high-frequency power supply noise from coupling into the signal path. Although the initial offset will be nulled to zero with this technique, issues of temperature drift must also be considered. The additional resistor R_3 is shown matched to the parallel combination R_1 and R_2 (the R_{TRIM} path is assumed to be negligible in this calculation). This will eliminate the first-order offset drift due to input bias current leaving only the input offset current (I_{OS}) drift multiplied by the feedback resistor R_2.

ESD PROTECTION

ESD damage has been a well recognized source of degradation for MOSFET type circuits, but any semiconductor device can be vulnerable to damage. This becomes more of an issue for very high speed processes like that used for the

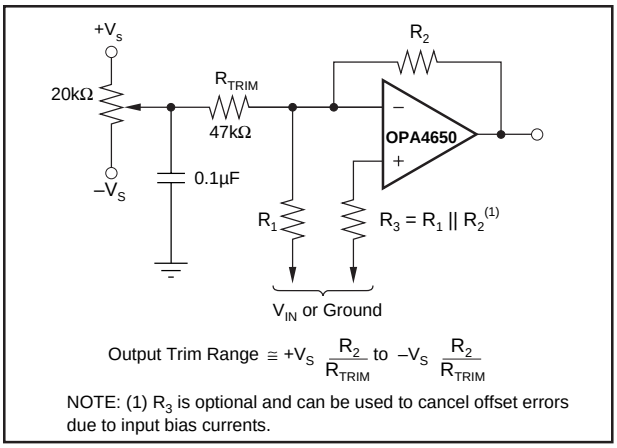


FIGURE 2. Offset Voltage Trim.

OPA4650. ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. ESD handling precautions are strongly recommended when handling the OPA4650.

OUTPUT DRIVE CAPABILITY

The OPA4650 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 1Vp-p into a 75Ω load. This high output drive capability makes the OPA4650 an ideal choice for a wide range of RF, IF and video applications. In many cases, additional buffer amplifiers are unnecessary.

Many demanding high speed applications, such as driving Analog-to-Digital converters, require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitance at the input of a flash A/D converter. As shown in Figure 3, the OPA4650 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing.

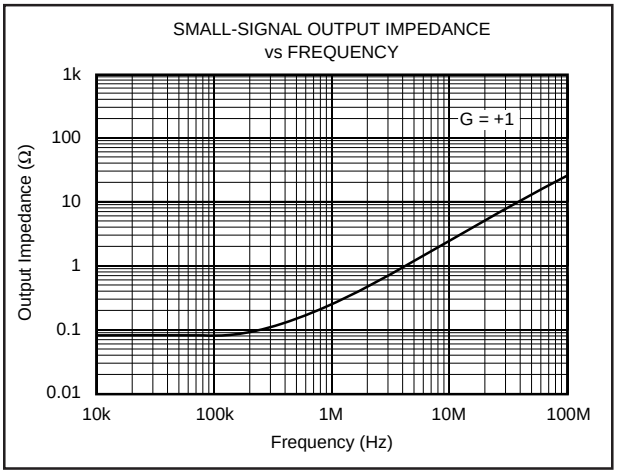


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA4650 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power for all channels (P_{DQ}) and the sum of the powers dissipated in each of the output stages (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is a fixed dc voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for an OPA4650U at A_V = +2, R_L = 100Ω, R_{FB} = 402Ω, $\pm V_S$ = ±5V, with all 4 outputs at $|V_S/2|$, and the specified maximum T_A = +85°C. P_D = 10V•35mA + 4•(5^2)/(4•(100Ω||804Ω)) = 631mW. Maximum T_J = +85°C + 0.641W•75°C/W = 133°C.

DRIVING CAPACITIVE LOADS

The OPA4650's output stage has been optimized to drive low resistive loads. Capacitive loads will decrease phase margin which may result in high frequency oscillations or peaking. Capacitive loads greater than 10pF should be isolated by connecting a small resistance (15Ω to 30Ω) in series with the output as shown in Figure 4. This is especially important when driving the capacitive input of high-speed A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/ft for RG-58) will not load the amplifier when the cable is source and load terminated in its characteristic impedance.

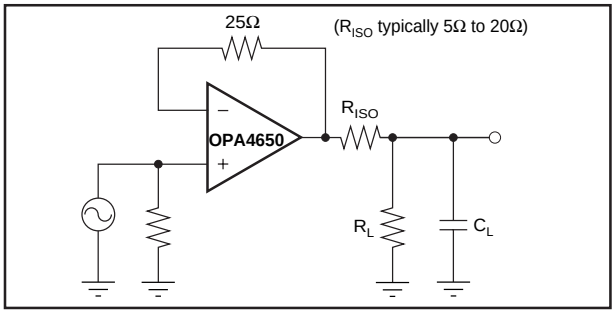


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

Each channel of the OPA4650 is internally compensated to be stable at unity gain with a nominal 60° phase margin. This lends itself well to wideband integrator and buffer applications. Phase margin and frequency response flatness will improve at higher gains. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes, i.e., noise gain = 2. The external compensation techniques developed for voltage feedback op amps can be applied to this device. For example, in the non-inverting configuration, placing a capacitor across the feedback resistor will reduce the gain to +1 starting at $f = (1/2\pi R_F C_F)$. Alternatively, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, thereby limiting the bandwidth for the inverting input signal through the gain-bandwidth product.

At higher gains, the gain-bandwidth of this voltage feedback topology will limit bandwidth according to the open-loop frequency response curve. For applications requiring a wider bandwidth at higher gains, consider the quad current feedback model, OPA4658. In applications where a large feedback resistor is required (such as photodiode transimpedance circuits), precautions must be taken to avoid gain peaking due to the pole formed by the feedback resistor and the summing junction capacitance. This pole can be compensated by connecting a small capacitor in parallel with the feedback resistor, creating a cancelling zero term. In other high-gain applications, use of a three-resistor "T" connection will reduce the feedback network impedance which reacts with the parasitic capacitance at the summing node.

PULSE SETTLING TIME

High speed amplifiers like the OPA4650 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a ±1V step at a gain of +1 for the OPA4650 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which isolates the output stage decoupling from the rest of the amplifier.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as DG. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. For the OPA4650, DG and DP are both specified at the NTSC color sub-carrier frequency of 3.58MHz and measured using industry standard video test equipment.

DISTORTION

The OPA4650's harmonic distortion characteristics for a 100Ω load are shown in the Typical Performance Curves. Distortion can be improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback network when calculating the effective load resistance seen by the amplifier.

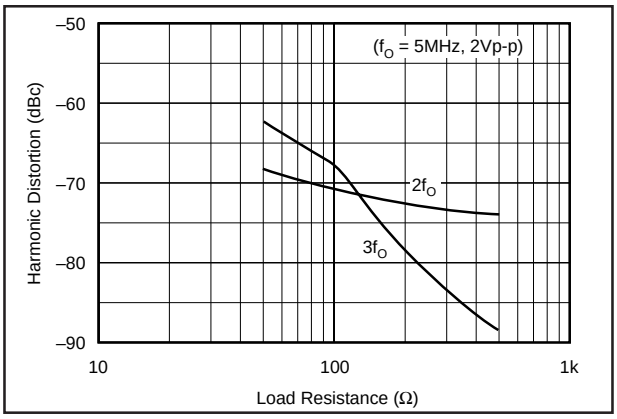


FIGURE 5. Harmonic Distortion vs Load Resistance.

CROSSTALK

Crosstalk is the undesired coupling of one channel's signal into the output of the other channels. Crosstalk is a consideration in all multichannel integrated circuits. The effect of crosstalk is measured by driving one ("channel-to-channel") or more ("all-hostile") channels and observing the output of the undriven channel. The magnitude of this effect is expressed in the crosstalk specification as decibels of gain. "Input referred" points to the fact that there is a direct correlation between gain and crosstalk, therefore output crosstalk increases proportionally at higher gains.

In quad devices, the effect of all-hostile crosstalk is observed by driving all three channels concurrently and measuring the output of the undriven fourth channel. The plots in Figure 6 illustrate both channel-to-channel and all-hostile crosstalk for the OPA4650.

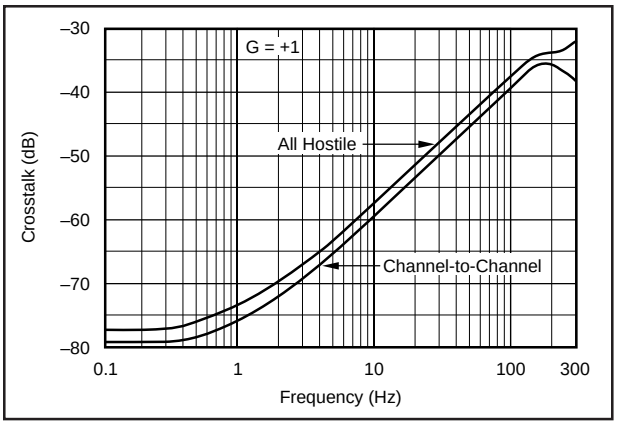


FIGURE 6. Channel-to-Channel Isolation and All Hostile Crosstalk.

NOISE FIGURE

The voltage and current noise spectral density are shown in the Typical Performance Curves. For RF and IF applications, however, Noise Figure (NF) is often the preferred specification. This specification shows a degradation in SNR through a device relative to the thermal noise of the source impedance alone.

The NF for the OPA4650, using 1MHz spot noise numbers and an unterminated non-inverting input, is shown in Figure 7.

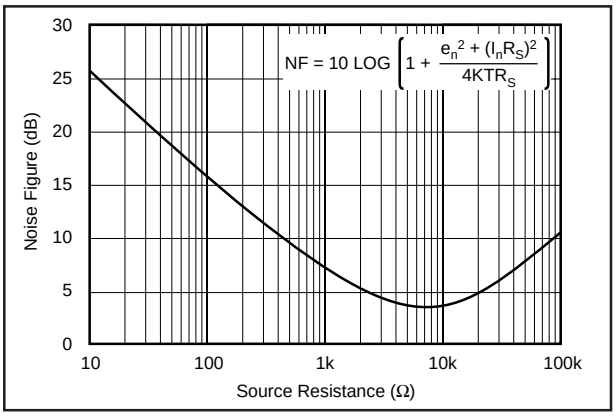


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS AND EVALUATION BOARD

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models and evaluation PC boards are available for the OPA4650. Contact the Burr-Brown Applications Department to receive a SPICE diskette.

DEMONSTRATION BOARD	PACKAGE	PRODUCT
DEM-OPA465xP DEM-OPA465xU	8-Pin DIP SO-8	OPA4650P oPA4650U

TYPICAL APPLICATION

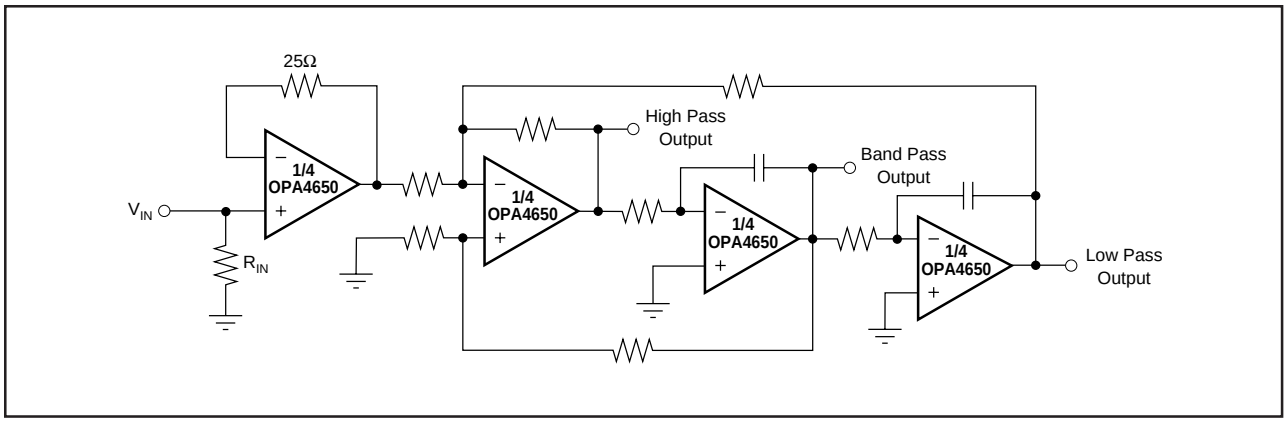


FIGURE 8. State-Variable Biquadratic Filter.

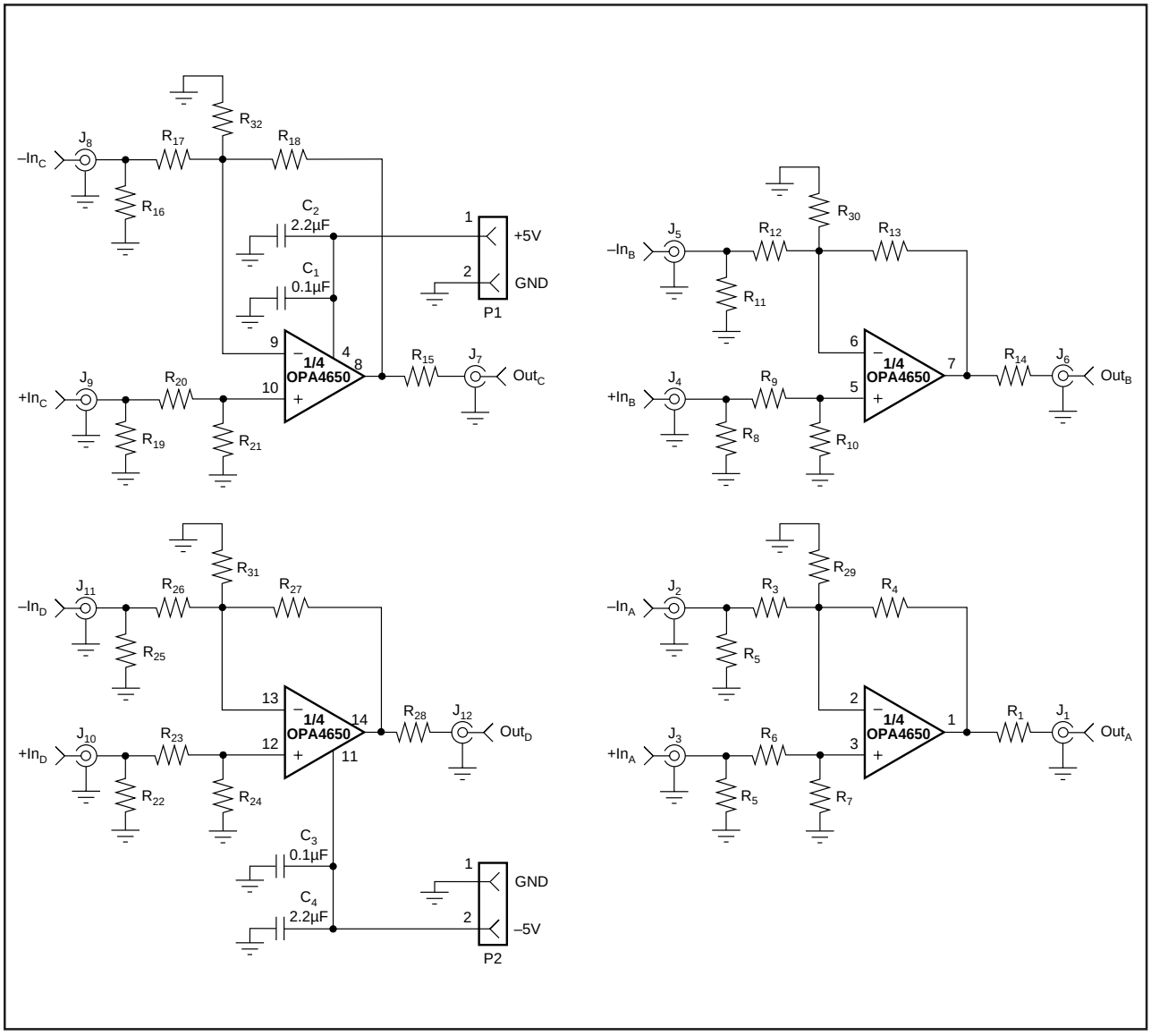
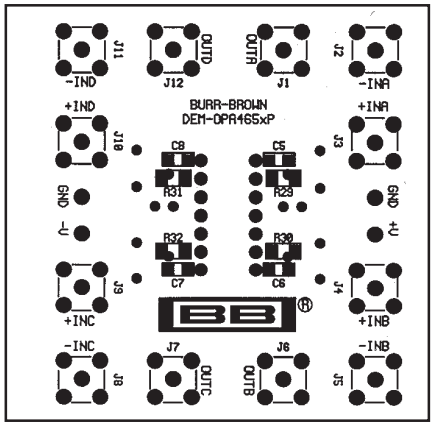
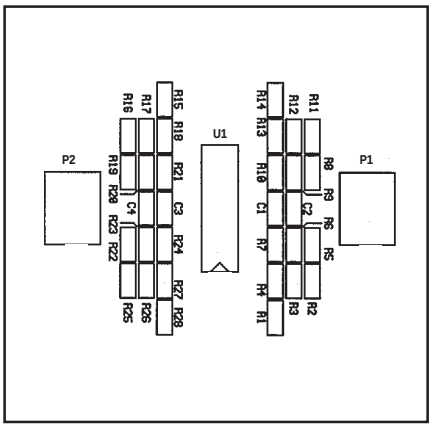


FIGURE 9. Circuit Detail for the DEM-OPA465xP Board.

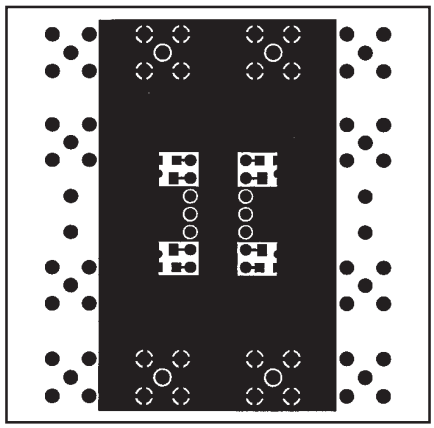
DEM-OPA465xP Demonstration Board Layout



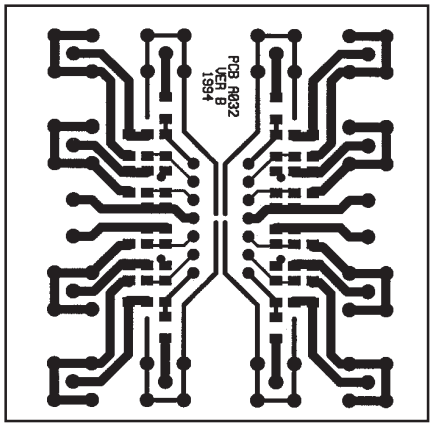
(A)



(B)



(C)



(D)

FIGURE 10a. Board Silkscreen (Bottom). 10b. Board Silkscreen (Top). 10c. Board Layout (Solder Side). 10d. Board Layout (Component Side).